Claims

1. (previously presented) An apparatus for displaying an image corresponding to a digital image file, comprising:

a) an image processing memory portion, the image processing memory portion including an image buffer for the computation of an image from a digital image file;

b) an integrated circuit in communication with the image processing memory portion, the circuit including integrated processing capability for the computation of the image from the digital image file;

c) a video memory portion in communication with the circuit, the video memory portion being capable of storing a plurality of computed images that are computed by the circuit; and

d) a direct memory access controller that is capable of providing efficient data transfer to or from media or interfaces that provide the digital image files to the apparatus, the image processing memory portion, the integrated circuit, and the video memory portion;

wherein the apparatus is further capable of inserting phase compensation pixels in between video frames so that an identical subcarrier phase is established in consecutive video frames.

2. (original) The apparatus of claim 1, further comprising a control processing unit that is capable of providing one or more of:

a) file system processing operations directed to a storage device or interface that provides the digital image file;

b) parsing, interpretation, and validation of compressed image file headers;

c) interpretation and execution of user commands; and

d) coordination of image processing operations of the integrated circuit.

3. (original) The apparatus of claim 1, further comprising a non-volatile memory portion that contains executable program code defining one or more operational characteristics of the apparatus or of a device into which the apparatus is incorporated, and that also contains one or more images used for informational or background display purposes.

4. (canceled)

5. (original) The apparatus of claim 1, further comprising one or more SDRAM controllers that provide control memory initialization, read and write cycles, and refresh operations.

6. (original) The apparatus of claim 1, further comprising at least one bus arbitration and multiplexing logic device that allows the image processing memory portion, the video memory portion, the integrated circuit, and file storage media to share one or more common signals.

7. (original) The apparatus of claim 1, wherein the integrated processing capability includes converting the digital image file into a viewable bitmapped image.

8. (original) The apparatus of claim 7, wherein the integrated processing capability further includes rescaling the viewable bitmapped image to fit an available viewing area of a television display.

9. (original) The apparatus of claim 7, wherein the integrated processing capability further includes filtering the viewable bitmapped image to reduce the severity of at least one television display artifact selected from the group consisting of cross-luminance, cross-chrominance, and video flicker.

10. (original) The apparatus of claim 7, wherein the integrated processing capability further includes converting the viewable bitmapped image into a television video signal.

11. (original) The apparatus of claim 1 further comprising an output that is capable of delivering any of the plurality of computed images to a display device without performing further digital computation.

12. (original) The apparatus of claim 11, wherein the processor is capable of providing time-multiplexed image data and one or more video synchronization signals to form a composite video signal.

13. (original) The apparatus of claim 1, wherein the integrated circuit is an application-specific integrated circuit or a field programmable gate array.

14. (original) The apparatus of claim 1, wherein the apparatus is further capable of decoding, storing, and providing informational or background images for delivery to a video output or display device.

15. (original) The apparatus of claim 1, wherein the circuit is further capable of transferring a computed image from the image processing memory portion to the video memory portion.

16. (previously presented) The apparatus of claim 15, wherein the circuit is further capable of delivering one or more synchronization pulses to a video output or display device via a video processor when the computed image is being transferred from the image processing memory portion to the video memory portion.

17. (canceled)

18. (original) The apparatus of claim 1 wherein the circuit is further capable of providing one or more of picture-in-picture video insertion, split-image display, and image transition effects.

19. (original) The apparatus of claim 1 wherein the circuit is further capable of providing an image navigation function, whereby the circuit increments or decrements an image index counter in response to user commands.

20. (original) The apparatus of claim 1 wherein the circuit is further capable of managing images cached in the video memory portion in a manner consistent with the direction of navigation as expressed by a user of the apparatus.

21. - 34. (canceled)

35. (previously presented) An apparatus for displaying an image corresponding to a digital image file, comprising:

a) an image processing memory portion, the image processing memory portion including an image buffer for the computation of an image from a digital image file;

b) an integrated circuit in communication with the image processing memory portion, the circuit including integrated processing capability for the computation of the image from the digital image file; and

c) a video memory portion in communication with the circuit, the video memory portion being capable of storing a plurality of computed images that are computed by the circuit; and

d) a control processing unit that is capable of providing one or more of:

1) file system processing operations directed to a storage device or interface that provides the digital image file;

2) parsing, interpretation, and validation of compressed image file headers;

3) interpretation and execution of user commands; and

4) coordination of image processing operations of the integrated circuit;

wherein the apparatus is further capable of inserting phase compensation pixels in between video frames so that an identical subcarrier phase is established in consecutive video frames.

36. (canceled)

37. (previously presented) The apparatus of claim 35, further comprising a non-volatile memory portion that contains executable program code defining one or more operational characteristics of the apparatus or of a device into which the apparatus is incorporated, and that also contains one or more images used for informational or background display purposes.

38. (previously presented) The apparatus of claim 35, further comprising one or more SDRAM controllers that provide control memory initialization, read and write cycles, and refresh operations.

39. (previously presented) The apparatus of claim 35, further comprising at least one bus arbitration and multiplexing logic device that allows the image processing memory portion, the video memory portion, the integrated circuit, and file storage media to share one or more common signals.

40. (previously presented) The apparatus of claim 35, wherein the integrated processing capability includes converting the digital image file into a viewable bitmapped image.

41. (previously presented) The apparatus of claim 40, wherein the integrated processing capability further includes rescaling the viewable bitmapped image to fit an available viewing area of a television display.

42. (previously presented) The apparatus of claim 40, wherein the integrated processing capability further includes filtering the viewable bitmapped image to reduce the severity of at least one television display artifact selected from the group consisting of cross-luminance, cross-chrominance, and video flicker.

43. (previously presented) The apparatus of claim 40, wherein the integrated processing capability further includes converting the viewable bitmapped image into a television video signal.

44. (previously presented) The apparatus of claim 35 further comprising an output that is capable of delivering any of the plurality of computed images to a display device without performing further digital computation.

45. (previously presented) The apparatus of claim 44, wherein the processor is capable of providing time-multiplexed image data and one or more video synchronization signals to form a composite video signal.

46. (previously presented) The apparatus of claim 35, wherein the integrated circuit is an application-specific integrated circuit or a field programmable gate array.

47. (previously presented) The apparatus of claim 35, wherein the apparatus is further capable of decoding, storing, and providing informational or background images for delivery to a video output or display device.

48. (previously presented) The apparatus of claim 35, wherein the circuit is further capable of transferring a computed image from the image processing memory portion to the video memory portion.

49. (previously presented) The apparatus of claim 48, wherein the circuit is further capable of delivering one or more synchronization pulses to a video output or display device via a video processor when the computed image is being transferred from the image processing memory portion to the video memory portion.

50. (previously presented) The apparatus of claim 35 wherein the circuit is further capable of providing one or more of picture-in-picture video insertion, split-image display, and image transition effects.

51. (previously presented) The apparatus of claim 35 wherein the circuit is further capable of providing an image navigation function, whereby the circuit increments or decrements an image index counter in response to user commands.

52. (previously presented) The apparatus of claim 35 wherein the circuit is further capable of managing images cached in the video memory portion in a manner consistent with the direction of navigation as expressed by a user of the apparatus.

53. (currently amended) ~~An apparatus for displaying an image corresponding to a digital image file, comprising:~~

~~a) an image processing memory portion, the image processing memory portion including an image buffer for the computation of an image from a digital image file;~~

~~b) an integrated circuit in communication with the image processing memory portion, the circuit including integrated processing capability for the computation of the image from the digital image file;~~

~~c) a video memory portion in communication with the circuit, the video memory portion being capable of storing a plurality of computed images that are computed by the circuit; and~~

The apparatus of claim 55 further comprising:

~~d)~~ e) a non-volatile memory portion that contains executable program code defining one or more operational characteristics of the apparatus or of a device into which the apparatus is incorporated, and that also contains one or more images used for informational or background display purposes~~;~~

~~wherein the apparatus is further capable of inserting phase compensation pixels in between video frames so that an identical subcarrier phase is established in consecutive video frames~~.

54. (currently amended) ~~An apparatus for displaying an image corresponding to a digital image file, comprising:~~

~~a) an image processing memory portion, the image processing memory portion including an image buffer for the computation of an image from a digital image file;~~

~~b) an integrated circuit in communication with the image processing memory portion, the circuit including integrated processing capability for the computation of the image from the digital image file;~~

~~c) a video memory portion in communication with the circuit, the video memory portion being capable of storing a plurality of computed images that are computed by the circuit; and~~

The apparatus of claim 55 further comprising:

~~d)~~ e) one or more SDRAM controllers that provide control memory initialization, read and write cycles, and refresh operations~~;~~

~~wherein the apparatus is further capable of inserting phase compensation pixels in between video frames so that an identical subcarrier phase is established in consecutive video frames~~.

55. (previously presented) An apparatus for displaying an image corresponding to a digital image file, comprising:

a) an image processing memory portion, the image processing memory portion including an image buffer for the computation of an image from a digital image file;

b) an integrated circuit in communication with the image processing memory portion, the circuit including integrated processing capability for the computation of the image from the digital image file;

c) a video memory portion in communication with the circuit, the video memory portion being capable of storing a plurality of computed images that are computed by the circuit; and

d) at least one bus arbitration and multiplexing logic device that allows the image processing memory portion, the video memory portion, the integrated circuit, and file storage media to share one or more common signals;

wherein the apparatus is further capable of inserting phase compensation pixels in between video frames so that an identical subcarrier phase is established in consecutive video frames.

56. (currently amended) ~~An apparatus for displaying an image corresponding to a digital image file, comprising:~~

~~a) an image processing memory portion, the image processing memory portion including an image buffer for the computation of an image from a digital image file;~~

~~b) an integrated circuit in communication with the image processing memory portion, the circuit including integrated processing capability for the computation of the image from the digital image file; and~~

~~c) a video memory portion in communication with the circuit, the video memory portion being capable of storing a plurality of computed images that are computed by the circuit;~~

~~wherein the apparatus is further capable of inserting phase compensation pixels in between video frames so that an identical subcarrier phase is established in consecutive video frames; and~~

The apparatus of claim 55 wherein the integrated processing capability includes converting the digital image file into a viewable bitmapped image.

57. (previously presented) The apparatus of claim 56, wherein the integrated processing capability further includes rescaling the viewable bitmapped image to fit an available viewing area of a television display.

58. (previously presented) The apparatus of claim 56, wherein the integrated processing capability further includes filtering the viewable bitmapped image to reduce the severity of at least one television display artifact selected from the group consisting of cross-luminance, cross-chrominance, and video flicker.

59. (previously presented) The apparatus of claim 56, wherein the integrated processing capability further includes converting the viewable bitmapped image into a television video signal.

60. (currently amended) ~~An apparatus for displaying an image corresponding to a digital image file, comprising:~~

~~a) an image processing memory portion, the image processing memory portion including an image buffer for the computation of an image from a digital image file;~~

~~b) an integrated circuit in communication with the image processing memory portion, the circuit including integrated processing capability for the computation of the image from the digital image file; and~~

~~c) a video memory portion in communication with the circuit, the video memory portion being capable of storing a plurality of computed images that are computed by the circuit;~~

~~wherein the apparatus is further capable of inserting phase compensation pixels in between video frames so that an identical subcarrier phase is established in consecutive video frames; and~~

The apparatus of claim 55 wherein the circuit is further capable of providing an image navigation function, whereby the circuit increments or decrements an image index counter in response to user commands.